

ENCAPSULATED OPTICAL PACKAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is the first application filed for the present invention. This application is related to commonly assigned co-pending applications filed herewith bearing agent docket numbers 16005-1US titled "Optical Connector Assembly" and 16005-2US titled "Optical Ferrule", the specifications of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] This invention relates to the field of optical packages. More precisely, this invention pertains to the field of packaging and coupling an optoelectronic chip, namely the encapsulation of optoelectronic devices and the provision for creating an optically flat and transparent window above the active region(s) of the optoelectronic device.

BACKGROUND OF THE INVENTION

[0003] Optoelectronic systems are increasing in their application to electronic equipment. High performance computers and computer network components increasingly involve conversion of computer data signals to photonic signals for transmission from one device to another, while such photonic signals require conversion to electronic data signals for use in the recipient electronic device.

[0004] Coupling optoelectronic components to waveguides remains an awkward aspect of manufacturing optoelectronic systems. Optoelectronic components are manufactured as small as possible, and therefore coupling requires precision alignment of components to waveguides. At the same time, waveguides such as optical fibers are very fragile and require secure encapsulation for mechanical stability and endurance. It is also difficult to achieve such requirements while keeping the resulting volume of a coupling as small as possible, a parameter that can be very important, if not essential, in many applications.

[0005] The encapsulation of microelectronic chips is very well known in the art and is commonly used to protect microchips in all varieties of chip packages. The method commonly used is to use a plastic resin and drop a glob of the resin over the wirebonded microchip within its package. US Patent 4,819,041 granted April 4, 1989 and US Patent 5,313,365 granted May 17, 1994 both are good examples of methods used to encapsulate microchips within specific packages. These methods use types of plastic resins to fill a cavity where the microchip has been placed with (typically) opaque resin and without any consideration for the surface profile of the resin. Other examples in the prior art describe transparent epoxies such as US Patent 6,075,911 granted June 13, 2000 and US Patent 6,269,209 granted July 31, 2001 are examples of transparent epoxy or silicon are used with optoelectronic device and optical fibers. These patents describe how the two elements are aligned and then subsequent to the alignment how the epoxy or silicon is injected between the optoelectronic device and the optical fiber to increase coupling and provide protection.

[0006] There are several prior-art references that are still patent pending that describe encapsulation of optoelectronics. US patent application Pub. No. US 2002/0001869 dated January 3, 2002 describes an encapsulation technique that uses a sacrificial layer over the encapsulated optoelectronic and includes methods for placing lenses over the open window, but does not describe a polishing method to reduce the thickness of the encapsulation, nor is alignment an issue. US patent application Pub. No. US 2002/0020803 dated February 21, 2002 describes a method of encapsulating an entire photodetector and support electronics in an over-molded type transparent resin that includes an embedded lens that allows for light to pass through the resin to the optoelectronic device. This prior-art also does not allow for 2-D alignment and does not include polishing to create the window. Finally, US patent application Pub. No. US 2002/0181899 dated December 5, 2002 discusses a method for imprinting a flat, but angled surface, on a transparent epoxy resin that encapsulated an optoelectronic device. The alignment method requires dowel pin alignment and is not amenable to polishing or 2-D alignment.

SUMMARY OF THE INVENTION

[0007] It is an object of the invention to provide a method for providing an encapsulated optoelectronic device.

[0008] According to a general aspect of the present invention, there is provided an assembly that can be treated the same way as other packaged microchips (for example: the placement of packaged chips on printed circuit boards) by encapsulating the optoelectronic device to form a complete package. However, the main reason for the requirement of a flat, transparent window over the optoelectronic device package is to provide the possibility for coupling other optical devices (such as optical fibers) to the optoelectronic device. The flat, transparent window facilitates the alignment procedure used between the optoelectronic device package and a second assembly (fiber optic ferrule, lens array, laser, etc.). The second assembly can be placed on the flat surface and aligned to the optoelectronic with a maximum of 3-degrees of movement required (2-lateral and 1-rotational). This methodology is known as stackable (or 2-D) optics, and greatly simplifies the alignment procedure. A specific example of this alignment strategy involves a vertical cavity surface emitting laser (VCSEL) array chip with an array of linear parallel optical fibers. Once the VCSEL array chip has been encapsulated in a transparent resin, it has a window (or flat, transparent surface) created above the array of Lasers on the VCSEL chip. The surface is essentially co-planar with the surface of the VCSEL chip. The distance between the surface of the VCSEL chip and the flat, transparent surface is kept to a minimum, without exposing the VCSEL chip, so that a maximum amount of coupling into optical fibers is possible.

[0009] This arrangement offers several other beneficial aspects as well. The encapsulated optoelectronic device is hermetically sealed so that no moisture or contaminants can develop over the device. It is also more resilient to vibration, especially if wirebonding is used to connect to the optoelectronic device. The transparent resin can also reduce the divergence of the light emitted from the optoelectronic device (assuming a high index of refraction epoxy is used for the

desired wavelength of light) and thereby allow for a longer physical distance for the same optical distance that the light can travel.

[0010] According to another aspect of the invention, there is provided a method for manufacturing an encapsulated optoelectronic package comprising an optoelectronic chip, comprising providing a substrate, securing an optoelectronic chip on the substrate, providing a translucent coating substance over the optoelectronic chip, and polishing the translucent coating substance to create planar surface over at least the optoelectronic chip, substantially parallel to the substrate, wherein the planar surface over the optoelectronic chip provides an optical coupling window.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Further features and advantages of the present invention will become apparent from the following detailed description, taken in combination with the appended drawings, in which:

[0012] Figs. 1a,b are a 3D perspective view and a top view of a substrate; the substrate comprises conductive trace lines and a location for receiving an optoelectronic chip;

[0013] Fig. 1c is a 3D perspective view of a standard Ceramic-Pin Grid Array (C-PGA) carrier with an optoelectronic device and transparent epoxy deposited in the open cavity;

[0014] Fig. 1d is a 3D perspective view of a custom carrier with the optoelectronic device on a separate block and a printed circuit board adjacent to the optoelectronic device;

[0015] Figs. 2a,b are a 3D perspective view and a top view of a substrate where an optoelectronic chip has been secured using electrically conductive epoxy;

[0016] Figs. 3a,b are a 3D perspective view and a top view of a substrate where a bump of transparent epoxy has been placed over the secured optoelectronic chip;

[0017] Fig. 4a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where the bump of epoxy has been polished over said optoelectronic chip;

[0018] Fig. 5 is a diagram which shows a geometric determination of maximum polish height;

[0019] Figs. 6a,b a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where a protection plate surrounding the optoelectronic chip has been placed;

[0020] Figs. 7a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where the protection plate surrounding the optoelectronic chip has been placed together with epoxy;

[0021] Figs 8a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where the protection plate surrounding the optoelectronic chip has been placed together with polished epoxy; and

[0022] Figs. 9a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip with an optional removal of the protection plate.

[0023] Fig. 10a is a 3D perspective view of a optical ferrule over the packaged optoelectronic chip;

[0024] Fig. 10b is a 3D perspective view of a metallic layer coated over the optical ferrule and packaged optoelectronic chip;

[0025] Fig. 10c is a 3D perspective view of a plastic protection resin (glob-top) over the metal coated optical ferrule and packaged optoelectronic chip;

[0026] It will be noted that throughout the appended drawings, like features are identified by like reference numerals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0027] The encapsulated optical package provides a simple method of producing an optical quality flat window over the active region of an optoelectronic device. The optical window is created perpendicularly to the direction of light emission/detection of the optoelectronic device.

[0028] In the case of an array of surface-emitting lasers, such as vertical cavity surface emitting laser (VCSEL) array chip, the window is created over the chip and is co-planar with the chip.

[0029] The optical window allows a method of alignment that eliminates several undesirable degrees of mechanical freedom. The flat, co-planar window restricts alignment to 2 lateral movements and one rotational movement (X , Y and \square_z). Typically, there are 6 degrees of mechanical movement (X , Y , Z , \square_x , \square_y , \square_z).

[0030] Electrical trace lines that extend from the encapsulated optoelectronic device to an external electrical connection, such as bond-fingers or a press-fit connector, provide the electrical access to the optoelectronic device.

[0031] In some embodiments, the optoelectronic device is first bonded onto the substrate using an electrically and thermally conductive epoxy. The exact placement of the optoelectronic chip with respect to the substrate can be done with low positional accuracy. It is one aspect of this invention that allows the subsequent alignment of optical fibers, lenses, or other optical components to the packaged optoelectronic device to be the critical alignment step for both the lateral and rotational position. Once optical fibers, lenses, or other optical components are aligned and fixed over the packaged optoelectronic device, the far-end of the optical fibers, lenses, or other optical components becomes the optical reference

surface and the electrical connections on the substrate must accommodate any positional error.

[0032] This packaging method also hermetically seals the optoelectronic chip so that it is not susceptible to humidity. Also, since the chip is encapsulated, its tolerance to mechanical vibration is greatly increased.

[0033] By encapsulating using a transparent material with a high refractive index, the divergence angle of the light-emitting device is decreased, allowing for a better coupling efficiency.

[0034] First preferred embodiment – polished transparent epoxy

[0035] As shown in figures 1a and 1b, the substrate (2) is the mechanical support for the assembly. It carries all of the elements and is used to electrically access the optoelectronic chip. There are many possible configurations for the chip carrier. The first is to use off-the-shelf pin grid array (PGA) chip carriers that have an inner cavity where the optoelectronic is placed and outer connection pins which are plugged into the PCB as shown in **figure 1c**. Transparent epoxy would be placed in the inner cavity over the optoelectronic chip and then polished flat. A second version, as shown in **figures 1a and 1b** is a more custom approach and could be based on patterning gold on an alumina substrate. A thin gold layer can typically be deposited on a flat aluminum oxide wafer or chip onto which the optoelectronic can be glued and wirebonded. As implied in the preferred embodiment, the external electrical connections to this custom-made chip carrier would allow, preferably, a second set of wirebonds from the substrate to an external PCB to take up the slack for any initial misalignment of the optoelectronic device with respect to the substrate. A third version is another custom approach that uses PCB technology and a small form connector to create the chip carrier as shown in **figure 1d**. The PCB (3) consists of trace lines (5) and a card-edge or similar electrical connection (7). The optoelectronic is placed on a metallic heat sink (9) over which the PCB is placed and bonded. The primary gain of this type of carrier is its adaptable

geometry and its heat-sinking capabilities. The steps described below involving transparent epoxy and polishing could all be equally applied to any of these mentioned arrangements of chip packages.

[0036] In the following embodiment, the chip carrier will be based on the second version, as shown in **figures 1a,b**, described above based on the gold patterned alumina substrate. The Encapsulated Optical Package consists of 5 elements. The elements are described as a substrate (or carrier package), transparent epoxy, electrically conductive epoxy, wirebonds, and an optoelectronic chip.

[0037] The custom-made alumina substrate is on the order of 1.5-cm x 1.5-cm x 0.2-cm in size. The top of the alumina substrate is patterned with a set of parallel gold trace lines (**6**) that start near the center of the substrate and end near one side of the substrate. The rest of the substrate, outside the trace lines is patterned with a continuous layer of gold (**4**) with alignment marks (**8**) for the placement of the optoelectronic chip. Preferably, the gold thickness and quality is amenable to wedge or ball wirebonding. The trace lines are used to transmit electrical signals from the perimeter of the substrate to the middle of the substrate where the chip will be placed as shown in **figures 2a,b**.

[0038] The optoelectronic chip (**10**) is placed near the middle of the substrate on a portion of the gold layer, within a reasonable distance for wirebonding from the tips of the trace lines. The emitting device, such as a vertical cavity laser (**12**), or a detecting device, such as a photodetector, is oriented so that its direction of operation is normal to the substrate for vertical coupling of the light, although side-launched optoelectronic device may also be contemplated. The exact placement of the chip is not critical, as long as the chip can be properly wirebonded to the trace lines. The chip is epoxied in place using electrically conductive epoxy (**16**) and is then wirebonded to the trace lines. Preferably, the wirebonds (**14**) are made as flat as possible so that their peaks are no more than 30-40-microns above the surface of the chip. Since the chip is higher than the trace lines, low wirebonds will be possible. For simplicity, and for when the chip has a common cathode, or anode,

on its backside, the trace lines for the common, or ground, potential may be connected directly to the area below the chip as shown in **figures 2a,b**.

[0039] A transparent epoxy is then used that will harden using time, heat, or UV-light with a sufficiently high hardness factor so that it can be polished. Preferably, the epoxy has sufficient viscosity before being set so that it does not spread out over the surface too quickly. The following epoxies were found to be well suited to this application: Dymax (model: OP-4-20632), Dexter (model: Hysol CNB753-42) and Eques (model: UV Laquer 1322 000 40045). These epoxies do not limit this application but only serve as examples of epoxies that have shown good properties in terms of wavelength, hardness, durability and moisture resistance.

[0040] The epoxy is deposited carefully over the optoelectronic chip, so not to damage the wirebonds. Preferably, the epoxy forms a somewhat convex bump **(18)** over the optoelectronic chip that completely encapsulates both the chip and the wirebonds, as shown in **figures 3a,b**. Preferably, the epoxy does not cover the distant ends of the trace lines so that the chip can still be accessed electrically.

[0041] The whole package is then placed on a polishing machine so that the bump of epoxy faces the polishing paper. Preferably, standard lapping and polishing techniques are applied, including progressively finer grits of polishing paper, correct timing, appropriate slurry mixtures, and a method of holding the parts in a rigid manner. Preferably, the polishing is stopped before the wirebonds or optoelectronic chip are damaged and an optically flat window **(20)**, that is co-planar with the surface of the optoelectronic device and chip substrate is formed. A thin, transparent layer of epoxy will remain over the chip as shown in **figures 4a,b**.

[0042] The maximum distance above an optoelectronic chip before optical crosstalk would occur can be calculated, as shown in **figure 5**. For a light emitter such as a VCSEL, the epoxy index of refraction " n_e ", the pitch of the light emitting devices on the optoelectronic chip " p ", and the open-air full divergence angle " θ " in

radians of the light source determines the maximum usable height of the epoxy above the chip:

[0043] Max. height = $(p/2) * (1/\tan((\theta/2)/n_e))$

[0044] For example, if $p=250$ -microns, $\theta=28$ -degrees= 0.4887 -rad, and $n_e=1.5$, max. height is equal to 760.5 -microns. However, distances as low as 50 -microns are also desirable to couple the maximum amount of light into optical fiber.

[0045] Alternative embodiment – polished transparent epoxy with removable protection plate

[0046] To aid in the process of polishing the transparent epoxy and/or to aid in containing the epoxy within a more confined volume on the substrate (2) around the chip (10), an intervening step can be performed.

[0047] The chip carrier, the chip, and the wirebonds are identical to the first preferred embodiment. However, before the transparent epoxy is placed over the chip, a frame or protection plate can be introduced. The protection plate (22) would typically have a hole or notch such that when it was placed on the chip carrier, it would surround the optoelectronic chip and the wirebonds. As shown in **figures 6a,b**, the protection plate could be made of various materials (glass, plastic, etc.) and would offer protection to the optoelectronic chip during the polishing procedure.

[0048] The thickness of the protection plate could be chosen to be slightly higher than the optoelectronic chip and wirebonds, and be of a material that would polish less quickly than the transparent epoxy. This would help ensure that the optoelectronic chip was not damaged. Depending on the protection plate material, and the method of depositing the epoxy, the plate could be either removed, in some manner, or left in place. Preferably, the plate is also non-conductive or at least insulated from the trace lines on the substrate, and allows access to the distant ends of the trace lines for electrical access to the optoelectronic chip.

[0049] The transparent epoxy is then injected into the open hole, or notch, over the optoelectronic chip provided by the protection plate. Enough epoxy (24) is used to completely encapsulate the chip and form a rounded surface of epoxy that is higher than the protection plate as shown in **figures 7a,b**. The epoxy is then time, heat or UV cured.

[0050] The assembly is then placed up side down on a polishing machine so that the protection plate and the epoxy face the polishing surface. The epoxy is polished until it is level with the protection plate and an optically flat window (26), that is co-planar with the chip and the substrate, is formed over the optoelectronic chip. Preferably, standard lapping and polishing techniques are applied, including progressively finer grits of polishing paper, de-ionized water, correct timing, appropriate slurry mixtures, and a method of holding the parts in a rigid manner as shown in **figures 8a,b**.

[0051] The resulting effect is shown in **figures 9a,b**, when the protection plate is removed.

[0052] Assembly – Complete Encapsulation Methods:

[0053] Ultimately, the encapsulated optical package must be placed into a useful support structure that allows access to the optical input or output and the electrical input or output. This requires that the encapsulated optical package be itself packaged in a second tier package (such as a transceiver housing) that may involve further encapsulation for mechanical stability and to protecting the transparent epoxy from moisture absorption or other contaminates. A standard method for sealing transparent epoxies is proposed in US patent 6,269,209 and US patent 6,075,911, both use resin barriers over their transparent epoxies to eliminate moisture absorption.

[0054] Although these referenced US patents may serve to protect against moisture, in the above embodiments, the use of a sufficiently moisture resistant resin or epoxy is assumed. Such epoxies were outlined above.

[0055] However, further to this patent disclosure is a method that allows for moisture resistance, electromagnetic interference protection and mechanical stability over the encapsulated optical package.

[0056] As shown in **figure 10a**, an optical ferrule (**28**) (related to commonly assigned co-pending application filed herewith bearing agent docket number 16005-2US titled "Optical Ferrule") has been placed over the encapsulated optical package of **figure 8a**.

[0057] As shown in **figure 10b**, the area over the transparent epoxy where the 45-degree beveled optical fibers (**30**) exist has been coated with a metallic layer (**32**), preferably by selective masking and gold evaporation techniques, so that: 1) the transparent epoxy is protected from moisture, 2) the optoelectronic is electromagnetically shielded when the shield is grounded, and 3) a metallic mirror is formed over the beveled optical fibers to aid in optical reflection into the optical fiber.

[0058] Finally, the entire assembly is coated in a protective standard thermoplastic resin (**34**) to mechanically bond the parts within a larger assembly as shown in **figure 10c**.

[0059] The embodiments of the invention described above are intended to be exemplary only. The scope of the invention is therefore intended to be limited solely by the scope of the appended claims.